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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,888	08/30/2001	Konstantinos Manetakis	010186	2078

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Qualcomm Incorporated
Patents Department
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EXAMINER	
NGUYEN, LINH V	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,888	MANETAKIS, KONSTANTINOS	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's argument filed on 5/23/03. Claims 1 – 22 are pending on this application.

Response to Arguments

2. Applicant's arguments filed 5/23/05 have been fully considered but they are not persuasive.

With respect to claims 1 and 10, under remarks applicant reference to "Analog VLSI Signal processing: Why, Where and How:" at page 12 to disclose the translinear loop is understood to be, "the base-emitter junctions of an even number of transistor are connected in series, half of them in each direction..". Therefore the cited "753" of Lee does not teach the translinear loop as defined by the above "Analog VLSI Signal processing". Examiner is respectful agree that Lee does not teach the translinear loop as defined above. However, in claims 1 and 10 of applicant's invention, the first, second, third and four MOS transistors configured in a translinear loop are pointing to the transistors in Fig. 1 of applicant's disclosure. In Fig. 1, first, second, third and four (My, Mx+y, Mx, Mz) do not have the above translinear loop configuration as defined by "Analog VLSI Signal processing". Therefore, the configuration of translinear loop transistors (My, Mx+y, Mx, Mz) of invention is defined by the following limitation in the claim as follows: the first MOS device (My) carrying a first control current (y), the second

MOS device (Mx) carrying a second control current (x), the third MOS device (Mx+y) carrying a current (x+y) equal to the sum of the first and second control currents, and the fourth MOS device carrying a bias current (z).

As discussed above, the translinear loop of applicant's claimed invention does not configured as "Analog VLSI Signal processing: Why, Where and How:" above. Therefore, the transistors in translinear loop of invention are defined by the currents limitation in each transistors by the claim. Since Lee et al. from previous office action, meet all the currents limitation in all four transistors of claimed invention, as result the transistors of Lee et al. meet the definition of translinear loop of claimed invention.

Drawings

3. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 3, 8, 10, 11, 12, 17, 18, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. US. Patent No. 5,223,753.

6. Regarding to claim 1, 10, and 18, Fig. 2 et al. disclose a amplifier circuit comprising: first (1), second (2), third (3), and fourth (12,13) MOS transistor devices configured in a translinear loop (no metes and bounds because the claimed does not have any structures or elements to describing this configuration), the first MOS device carrying a first control current (out put current of 1), the second MOS device carrying a second control current (output current of 2), the third MOS device carrying a current (current going through 3)) equal to the sum of the first and second control currents, and the fourth MOS device carrying a bias current (IX, IY); a first output circuit (11) coupled to a first voltage supply (VSS) and (drain of 11), the first output circuit sourcing a first output current based on the first control current (current mirror of 1); and a second output circuit (10) coupled to a second voltage supply (VDD) and the output node, the second output circuit sourcing a second output current (current mirror of 2)) based on the second control currents (Current mirror I17, I18).

7. Regarding to claims 2 and 11, wherein the first and second output circuits are current mirrors and the first and second output currents equal the first and second control currents respectively (I10 current mirror of output current 2, I11 current mirror of output current 2).

8. Regarding to claims 3 and 12, wherein the MOS devices are NMOS devices (Fig. 2).

9. Regarding to claims 8 and 20, wherein a quiescent current of the Output stage is set by the bias control current (IX, IY), the bias current being increased above a selected predetermined level to lower a distortion level of the circuit (Col. 3 lines 65 – 68).

10. Regarding to claim 17,wherein the first and second output circuits comprise first and second output MOS devices, respectively, the maximum output voltage range at the output node being substantially equal to the difference between the first and second voltage supplies minus a saturation voltage of the first and second MOS output devices (inherent to Fig. 2).

11. Regarding to claim 19, wherein the source of the second MOS and third and MOS (2, 3) devices are coupled to a bias voltage (Vss, 3 directly connected to Vss, and 2 coupled to Vss through 3).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 4, and 13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. as applied to claim 1, and 10 above, and further in view of 6,437,612, or 6,414,552, or 5,631,607, or 5,856,749, or 5,734,297 or 5,561,396.

14. Regarding to claim 4, and 13, As discussed above Lee et al. disclose every aspect of applicant's claimed invention, but does not explicitly disclose wherein the MOS devices operate in weak inversion mode. However weak-inversion mode are well-known art and a matter of design choice to have MOS devices operate in weak-inversion mode as have taught by many cited arts indicated above. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have MOS devices of Lee et al. amplifier operate in weak-inversion mode, which has taught by '612' ----'906'.

15. Claims 5, 6, 9, 14, 15, 16, 21 and 22, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. as applied to claims 1, 8, 10, and 20 above.

16. Regarding to claims 5, 6, 14, 15, and 16, Lee et al. do not explicitly wherein further comprising a supply voltage having a voltage lower than 2 * VGS + VDS^{sat} to provide the first voltage supply, or a supply voltage having a voltage equal to VGS + 2* VDS^{sat} to provide the first voltage supply, or the first voltage supply is 1.8 volts and the second voltage supply is a ground reference. It would have been obvious to one having ordinary skill in the art at the time the invention was made to optimum value of the voltage supply, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

17. Regarding to claim 9, 21, and 22, Lee et al. do not explicitly disclose the output node is coupled to an audio circuit or a power control circuit.

It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. EX parte Masham, 2 USPQ2d 1647 (1987).

18. Claim 7, is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. as applied to claim 1 above, in view of Huijising et al. U.S. patent No. 5,486,790

Lee et al. do not disclose wherein the bias current is programmable to permit user selection of a bias current.

Huijising et al. teach an AB amplifier circuit having programmable control bias current (Col. 5 lines 49 – 50).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have bias current of Lee et al. 's amplifier programmable which has taught by Huijising et al for the purpose providing selection of bias currents (Col. 5 lines 49 – 50).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are (703-872-9306) for regular communications and (703-872-9306) for After Final communications.

LVN

03/29/05

Art 2819

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